

## IN THE CLAIMS

1. (Currently amended) Method for transmitting a vector, in a computer system comprising: a processor; a multi-port memory, which is accessible by the processor, characterized in that the method comprises the steps of: passing a base memory address to an address configuration means; defining a set of memory addresses by the address configuration means using the base memory address and a configuration instruction for configuring the address configuration means; transmitting the vector to/from the multi-port memory at one time using the set of memory addresses.

2. (Previously presented) Method according to claim 1, wherein: the address configuration means comprises: a plurality of register files being configured by the configuration instruction, and a plurality of address calculation units for calculating the set of memory addresses; the register files being accessible by the address calculation units; the address calculation units being coupled to the multi-port memory.

3. (Previously presented) Method according to claim 1, wherein: the configuration instruction comprises a set of offsets, each offset in combination with the base memory address defining a second memory address.

4. (Currently amended) A computer system comprising: a processor; a multi-port memory, the multi-port memory being accessible by the processor, characterized in that the computer system further comprises an address configuration means, wherein the address configuration means is conceived to define a set of memory addresses using a base memory address and a configuration instruction for configuring the address configuration means, and wherein the multi-port memory is conceived to use the set of memory addresses at one time.

5. (Previously presented) A computer system according to claim 4, wherein: the address configuration means comprises: a plurality of register files arranged to be configured by the configuration instruction, and a plurality of address calculation units for calculating

the set of memory addresses; the register files are accessible by the address calculation units; the address calculation units are coupled to the multi-port memory.

6. (Previously presented) A computer system according to claim 4, wherein: the configuration instruction comprises a set of offsets, each offset in combination with the base memory address defining a second memory address.

7. (Previously presented) A computer system according to claim 4 wherein the multi-port memory and the address configuration means are included in a memory system.

8. (Previously presented) A computer program comprising computer program code means for instructing a computer system to perform the steps of the method as claimed in claim 1.